REMARKS

Claims 1-4 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Figure 1d of the present application in view of Chen, *et al.* (U.S. Patent No. 6,033,950). Claims 5 and 6 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Figure 1d of the present application in view of Chen, *et al.* and further in view of Hanagasaki (U.S. Patent No. 5,767,541). In view of the amendments to the claims and the following remarks, the rejections are respectfully traversed, and reconsideration of the rejections is requested.

In the applicants' invention, a capacitor structure includes an upper electrode which includes a three-layer deposition structure. The three-layer structure includes a doped polysilicon layer between first and second undoped polysilicon layers. The upper undoped polysilicon layer is formed immediately adjacent to a metal layer used in forming the upper electrode of the capacitor. Undoped polysilicon is used as the upper layer interface with the metal layer to provide a thicker adhesion layer between the metal layer and the polysilicon to prevent lifting of the metal layer.

In contrast, in the structure illustrated in Figure 1d of the application and described in the applicants' Background of the Invention section, the polysilicon pattern in the capacitor electrode is a two-layer pattern which includes a lower undoped polysilicon layer and an upper doped polysilicon layer. A metal pattern is formed over the upper doped polysilicon. During subsequent processes such as an anealing process, a silicide layer is formed between the polysilicon layer and the metal layer, resulting in improved adhesion between the metal layer and the polysilicon. However, adhesion between the silicon and the metal layer is determined by the degree to which the metal and silicon react during anealing. The thickness of the resulting silicide layer is inversely proportional to the doping layer of the polysilicon in contact with the metal layer. Thus, the high impurity concentration in the polysilicon layer results in a relatively thinner silicide layer, which, in turn, results in reduced adhesion between the metal and the polysilicon.

Hence, the applicants' improvement over the prior art device involves reducing the impurities in the layer contacting the metal. This results in a thicker layer being formed between the two during the anealing process, which results in better adhesion.

In Chen, *et al.*, as the Examiner notes, an undoped polysilicon layer 34 is formed on a doped polysilicon layer 32 to form an electrode of a capacitor. The upper undoped polysilicon layer 34 is used to reduce out-diffusion of impurities from the lower doped polysilicon during thermal cycles, thus preventing auto doping. In auto doping, the dopant diffuses out of the polysilicon and reaches the surface of the device and diffuses into the substrate during subsequent thermal processes. In other devices formed on the same wafer, the out-diffused dopant laterally and vertically increase the other dopant concentrations near or under edges of channel regions of adjacent devices. The undoped polysilicon layer 34 is placed on top of the doped polysilicon layer 32 to prevent this out-diffusion of dopant.

In view of the drawbacks of the prior art device described by the applicants, there is no motivation found in either prior art device for combining the prior art device with Chen, *et al.* Chen, *et al.* does not suggest any motivation for adding an undoped polysilicon layer to the prior art device of Figure 1d. That is, one skilled in the art in possession of the teaching in connection with Figure 1d of the present application would in no way be motivated to use the teaching of Chen, *et al.* to solve the problem of adhesion of an upper metal layer, since Chen, *et al.* teaches an undoped polysilicon layer to prevent out-diffusion of dopants into the body of a device. Also, Chen, *et al.* does not at all contemplate adhesion of a metal layer, since the undoped polysilicon layer of Chen, *et al.* is adjacent to a thick insulating layer 40, not a metal conductive layer. Furthermore, neither reference provides any motivation for making such a combination since the drawbacks in the prior art device in Figure 1d would not in any way suggest a solution disclosed by Chen, *et al.*

The claims have been amended to specifically set forth a three-layer polysilicon structure including a doped polysilicon layer between first and second undoped polysilicon layers. Since there would be no motivation for one of skill in the art to combine the structure of Figure 1d of

the application with the teachings of Chen, *et al.* to obtain such a three-layer structure, it is believed that the rejection of the claims under 35 U.S.C. § 103(a) based on the combination of Figure 1d and Chen, *et al.* is improper. Accordingly, reconsideration of the rejections of the claims based on Figure 1d of the application, Chen, *et al.* and Hanagasaki is respectfully requested.

Attached hereto is a marked-up version of the changes made to the application by the current Amendment. The attached pages are captioned "Version with Markings to Show Changes Made."

In view of the foregoing remarks, it is believed that all claims pending in the application are in condition for allowance, and such allowance is respectfully solicited. If a telephone conference will expedite prosecution of the application, the Examiner is invited to telephone the undersigned.

Respectfully submitted,

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Version with Markings to Show Changes Made

Claim 1 has been amended as follows:

1. (Amended) A semiconductor capacitor having a lower electrode, a dielectric layer and an upper electrode, wherein the upper electrode comprises a deposition structure including three layers including a doped polysilicon layer formed between a first undoped polysilicon layer and a second undoped polysilicon layer.

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